Schematic Package Supplement to

FAST FREDDIE™

Operation, Maintenance and Service Manual

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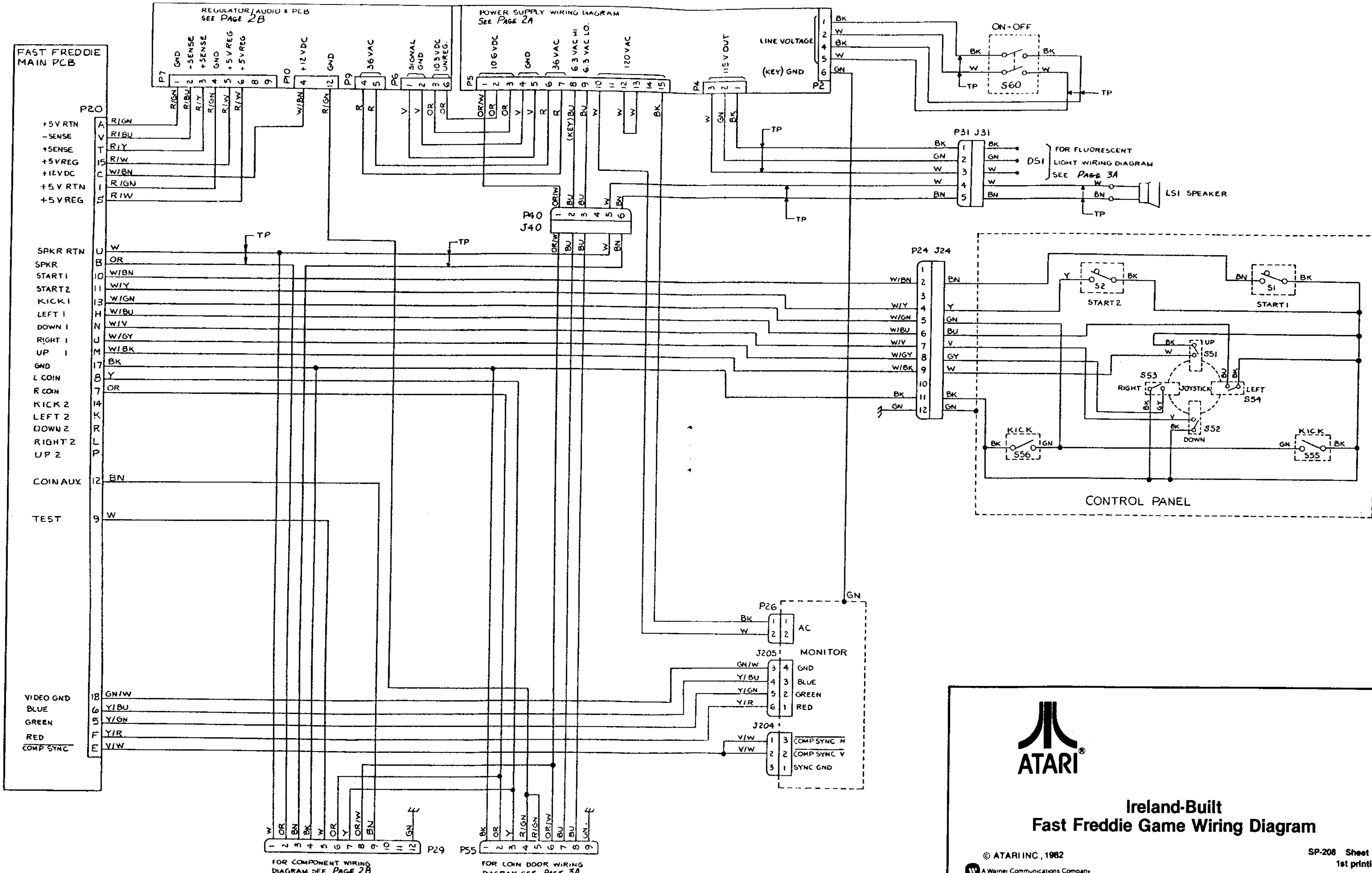
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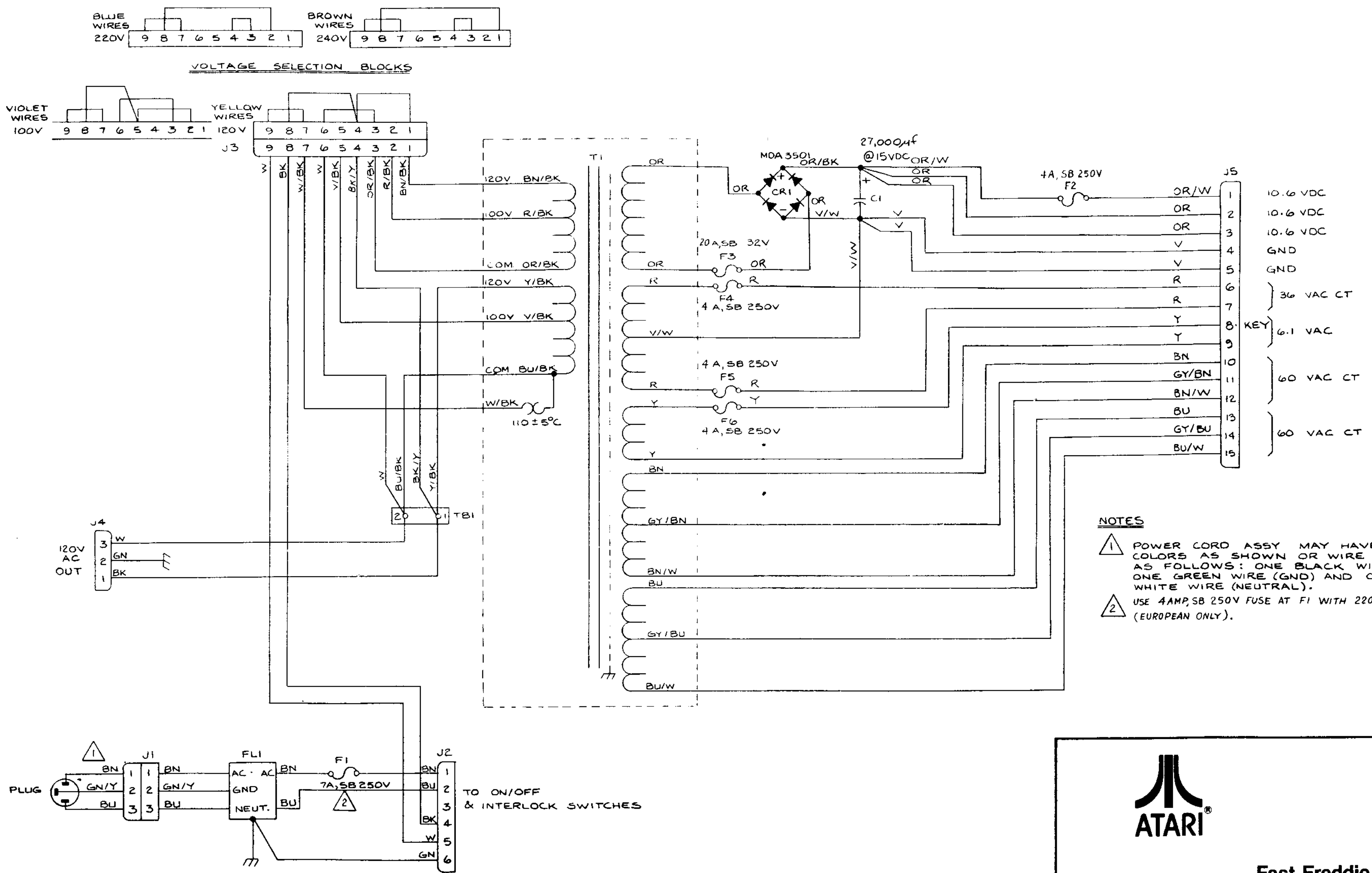
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Ireland-Built Fast Freddie Game Wiring Diagram

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NOTES

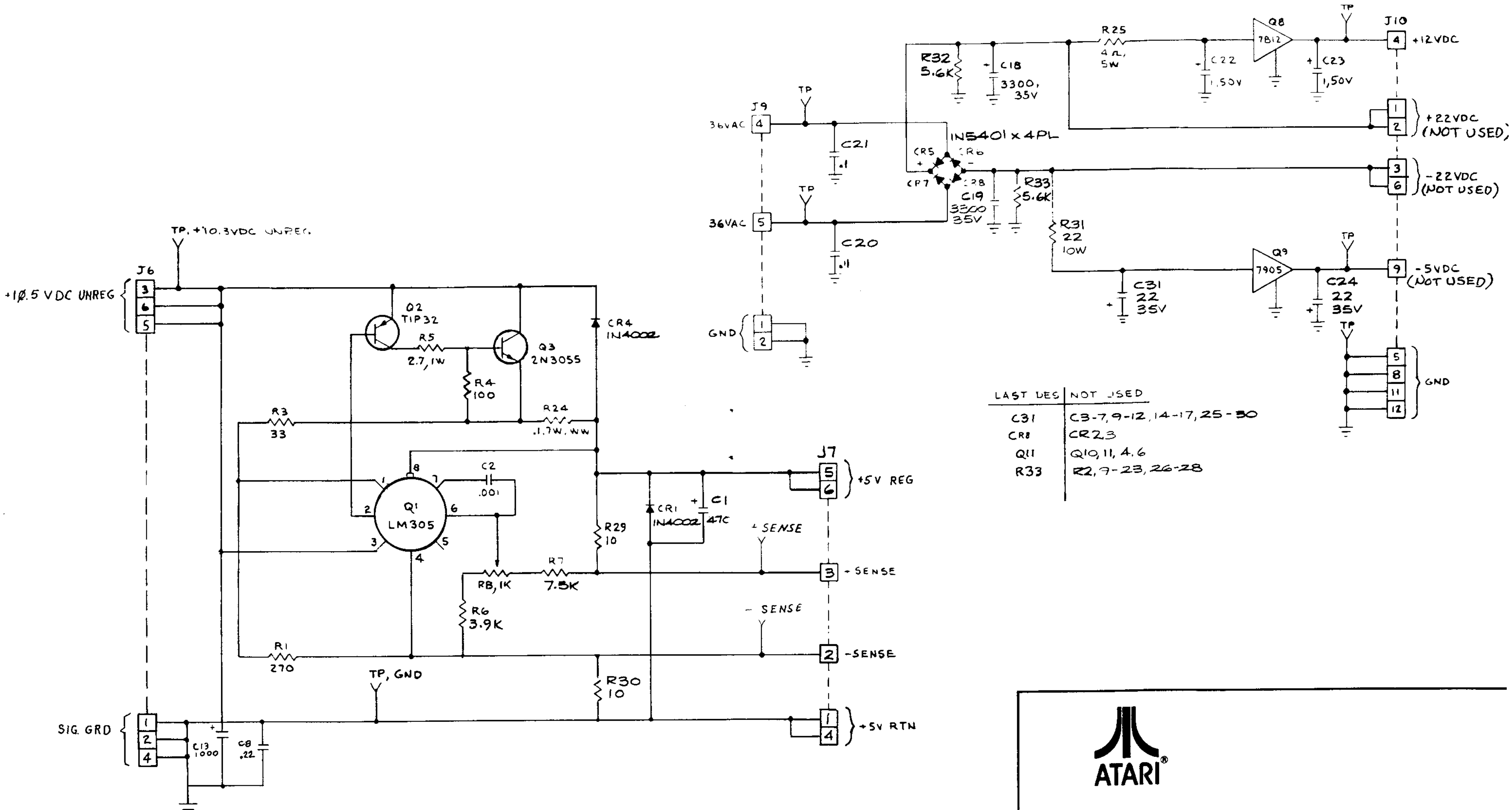
1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).

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Fast Freddie
Power Supply Wiring Diagram

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LAST DES	NOT USED
C31	C3-7, 9-12, 14-17, 25-30
CR8	CR23
Q11	Q10, 11, 4, 6
R33	R2, 9-23, 26-28

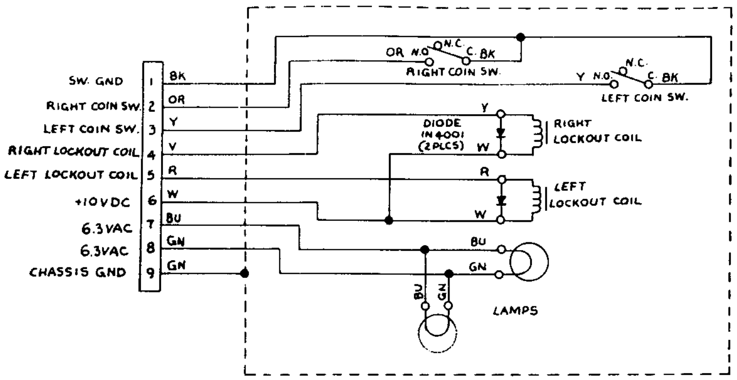
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Fast Freddie
Regulator/Audio II PCB Schematic

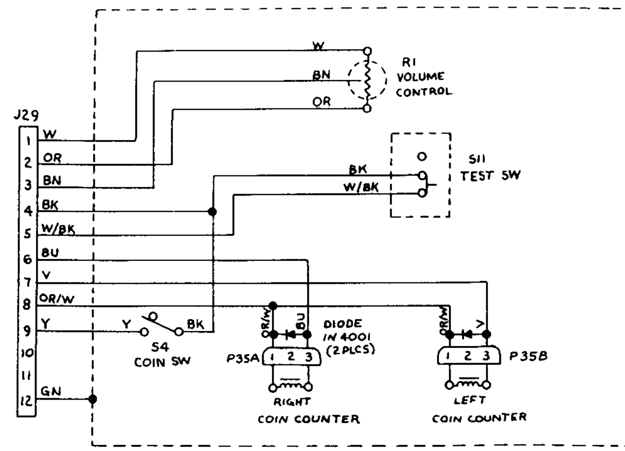
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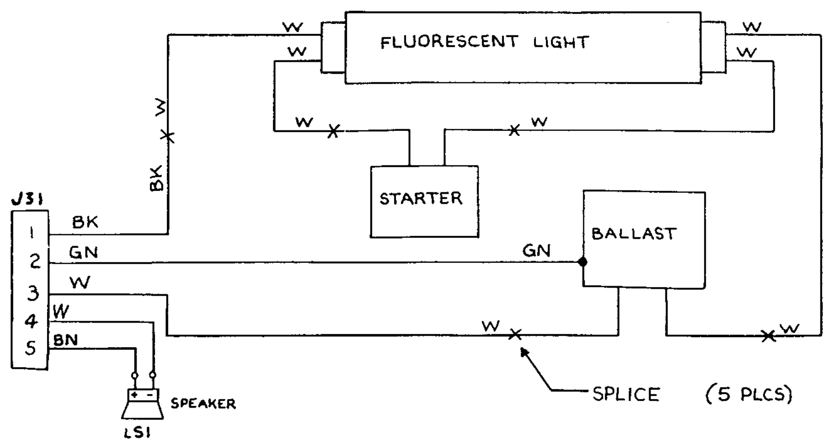
Coin Door Wiring Diagram



Utility Panel Wiring Diagram



Fluorescent Light and Speaker Wiring Diagram

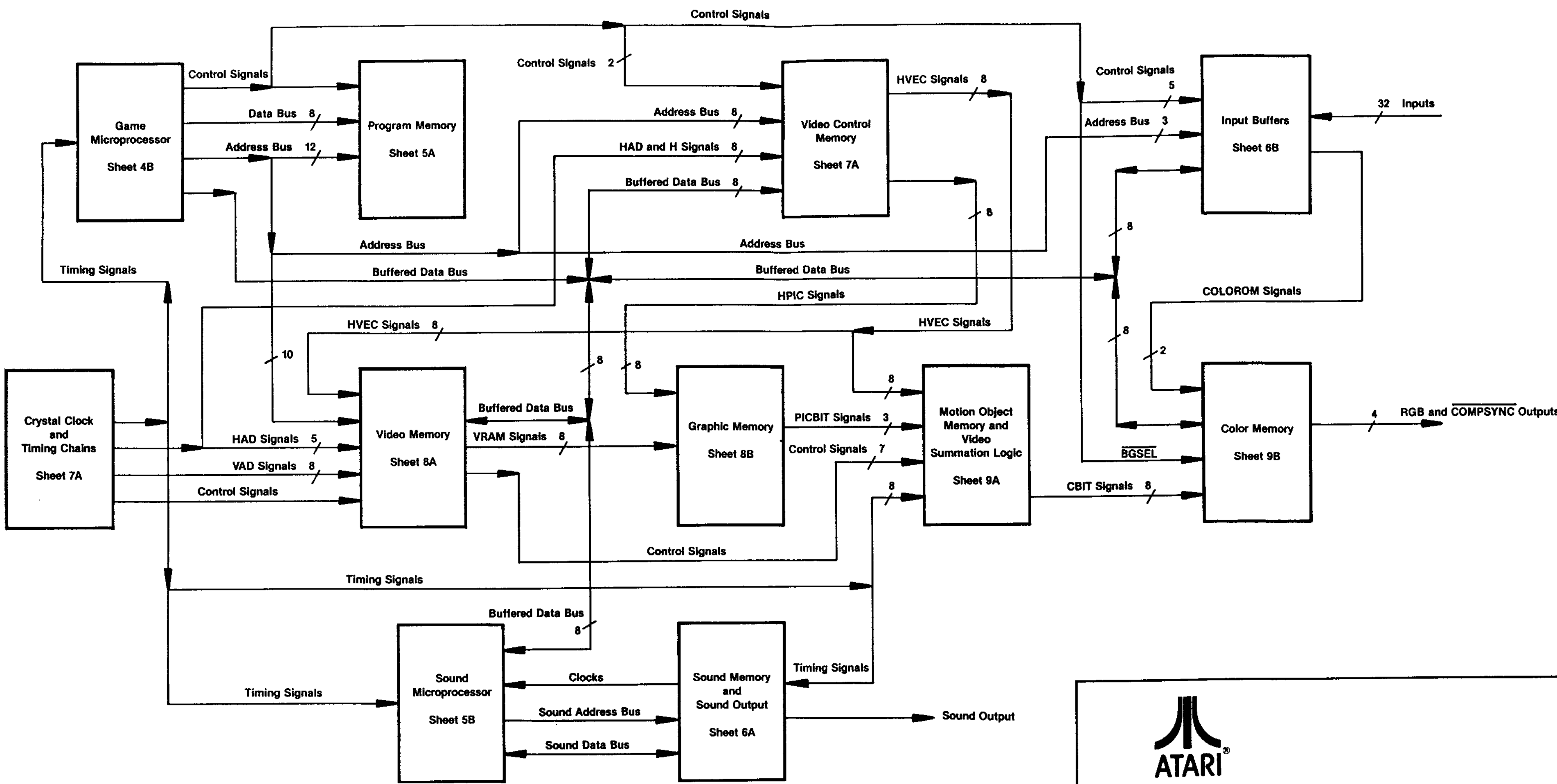


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Game Wiring Interfaces

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Fast Freddie
PCB Block Diagram

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Fast Freddie PCB Connector

Soldering Face			Parts Face
GND	A	1	GND
SP Out	B	2	No Connection
+ 12 V	C	3	+ 12 V
+ 12 V	D	4	+ 12 V
Sync	E	5	Green
Red	F	6	Blue
1 Player Left	H	7	Coin 2
1 Player Right	J	8	Coin 1
* 2 Player Left	K	9	Test
* 2 Player Right	L	10	1 Player Start
1 Player Up	M	11	2 Player Start
1 Player Down	N	12	Coin Aux. Input
* 2 Player Up	P	13	1 Player Kick
* 2 Player Down	R	14	* 2 Player Kick
+ 5 V	S	15	+ 5 V
+ 5 V	T	16	+ 5 V
GND	U	17	GND
GND	V	18	GND

* No connection in upright mode.

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Fast Freddie
Memory Map and PCB Connector

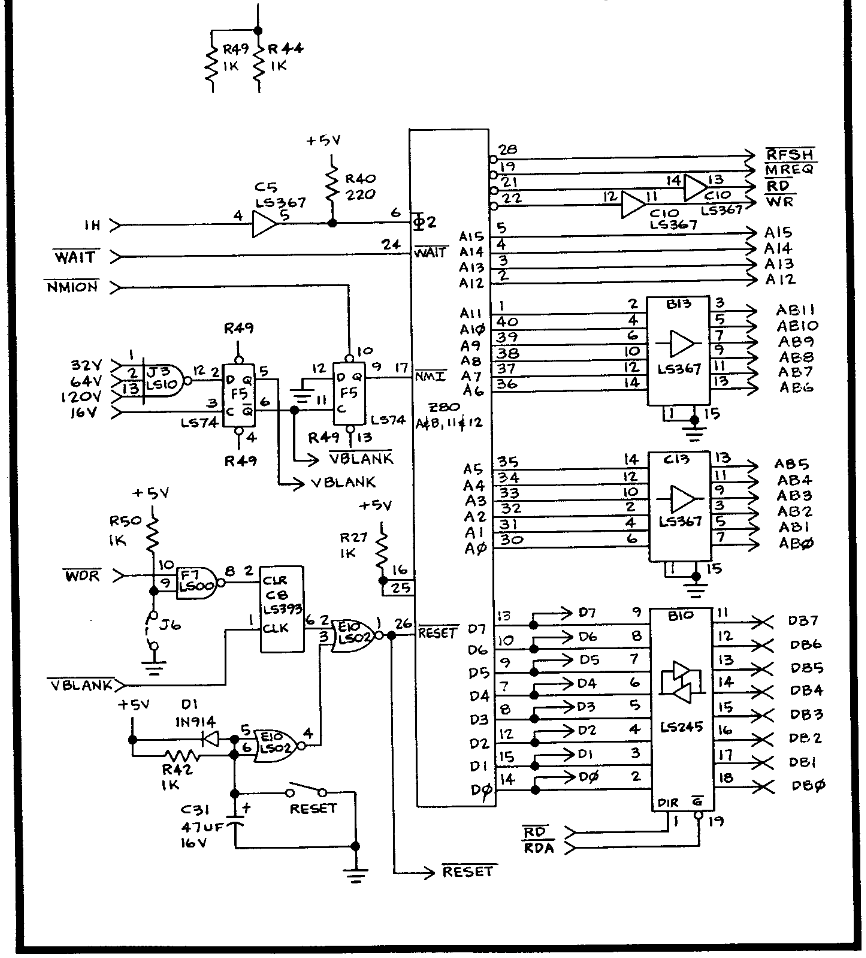
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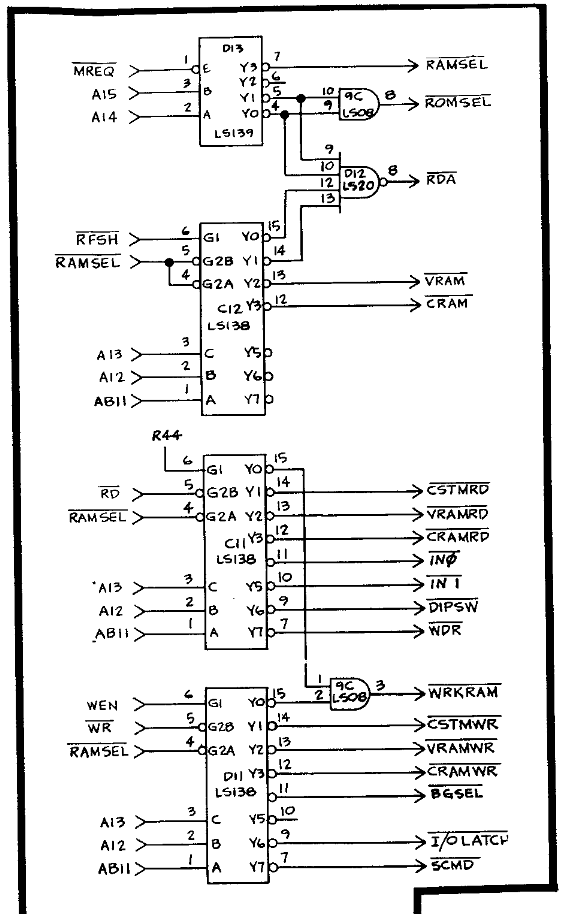
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MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Game Microprocessor Memory Space										
0000-7FFF	R	D	D	D	D	D	D	D	D	Z80 32K Program ROM
C000-C7FF	R/W	D	D	D	D	D	D	D	D	2K Working RAM
C800-C8FF	R/W	D	D	D	D	D	D	D	D	Custom Chip
D000-D3FF	R/W	D	D	D	D	D	D	D	D	1K Video RAM
D800-D8FF	R/W	D	D	D	D	D	D	D	D	Control RAM
E000	W	D	D	D	D	D	D	D	D	Background Color Select
E000	R								D	Coin 2
E000	R							D		Coin 1
E000	R						D			Test
E000	R					D				1 Player Start
E000	R				D					2 Player Start
E000	R			D						Coin Aux: Input
E000	D		D							1 Player Kick
E000	R	D								2 Player Kick
E800	R								D	1 Player Left
E800	R							D		1 Player Right
E800	R						D			2 Player Left
E800	R					D				2 Player Right
E800	R				D					1 Player Up
E800	R			D						1 Player Down
E800	R		D							2 Player Up
E800	R	D								2 Player Down
F000	R	D	D	D	D	D	D	D	D	Option Switch
F000	W								D	NMI Preset
F001	W								D	Character ROM Select 1
F002	W								D	Character ROM Select 2
F003	W								D	Color ROM Select 1
F004	W								D	Color ROM Select 2
F005	W								D	Horizontal Flip
F006	W								D	Vertical Flip
F800	W	D	D	D	D	D	D	D	D	Sound Output Port ($\overline{\text{SCMD}}$)
F800	R									Soft Reset
Sound Microprocessor Memory Space										
0000-1FFF	R	D	D	D	D	D	D	D	D	4K Sound Program ROM
2000-27FF	R/W	D	D	D	D	D	D	D	D	2K Sound Working RAM
3000	R	D	D	D	D	D	D	D	D	Input Port From Game C.P.U. ($\overline{\text{SCMDRD}}$)
3000	W								D	$\overline{\text{SNMI}}$ Preset
5000	W	D	D	D	D	D	D	D	D	Programmable Sound Generator
5001	W	D	D	D	D	D	D	D	D	Programmable Sound Generator
6000	W	D	D	D	D	D	D	D	D	Programmable Sound Generator
6001	W	D	D	D	D	D	D	D	D	Programmable Sound Generator

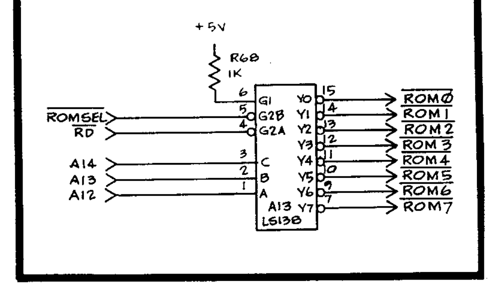
Game Microprocessor





Game Microprocessor Address Decoders

ROM Decoder



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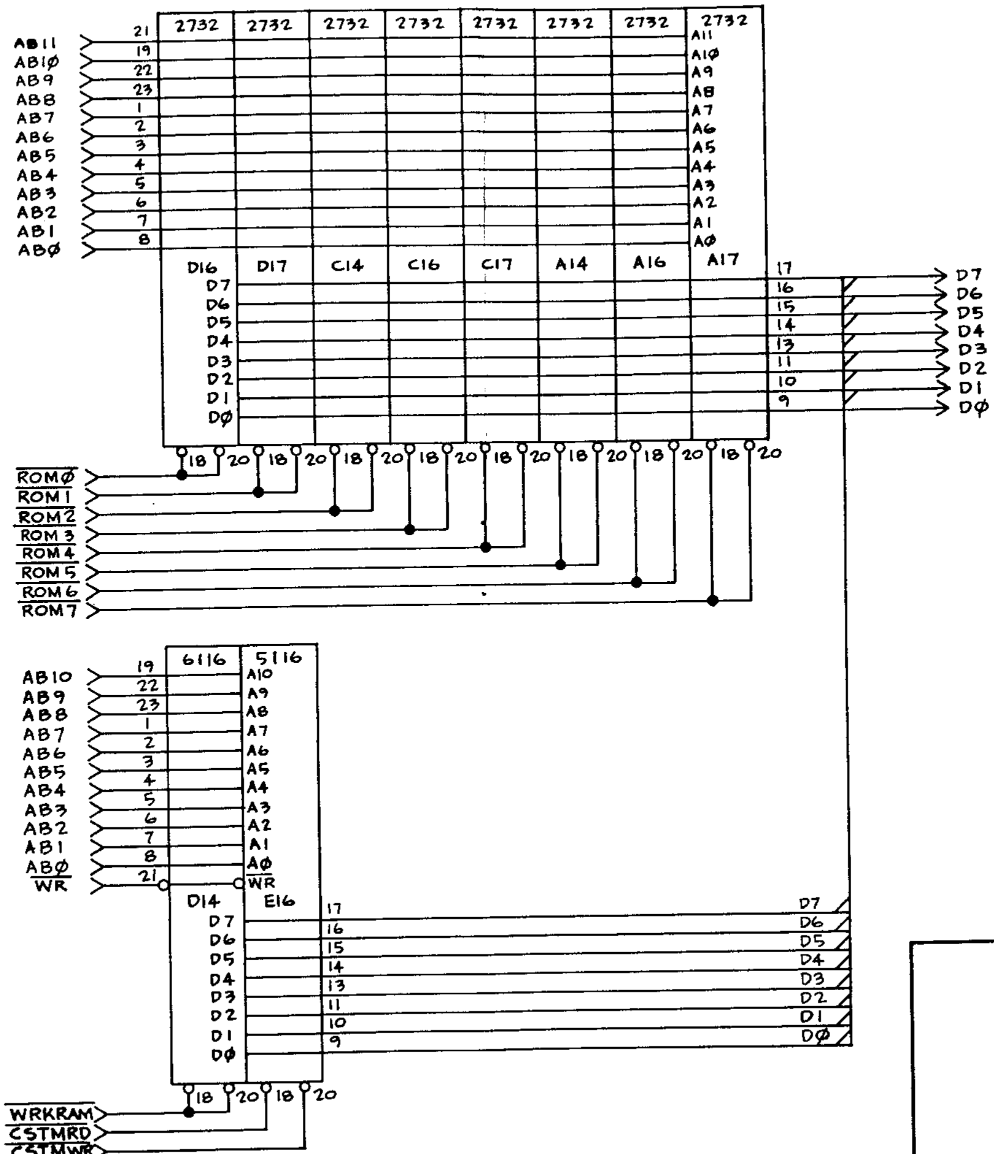
Fast Freddie
Game Microprocessor and Decoders

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Program Memory



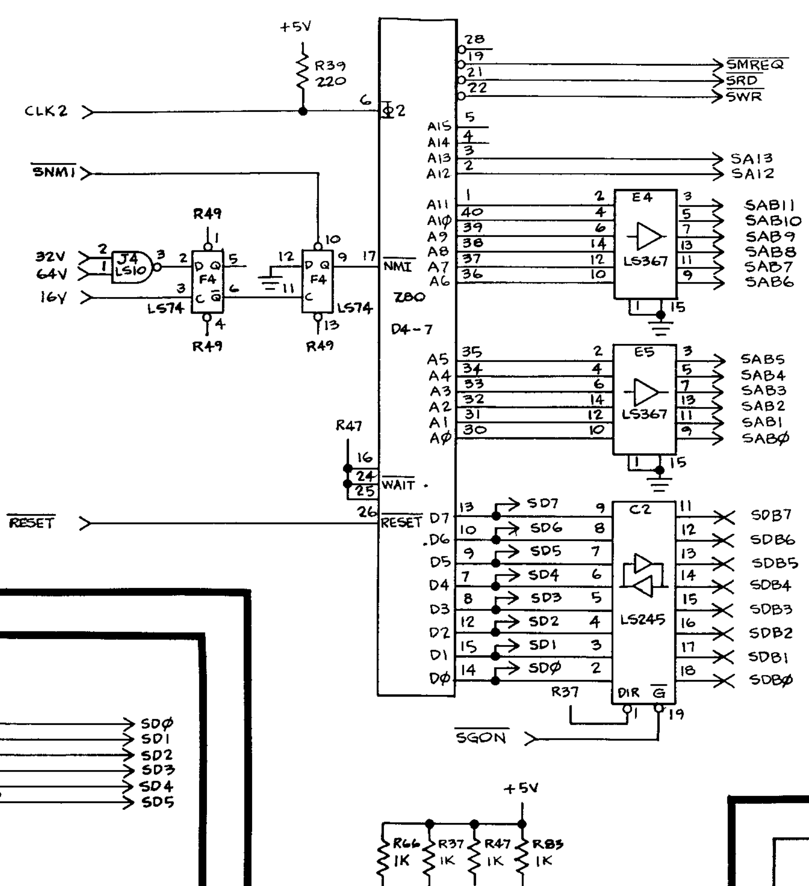
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Program Memory

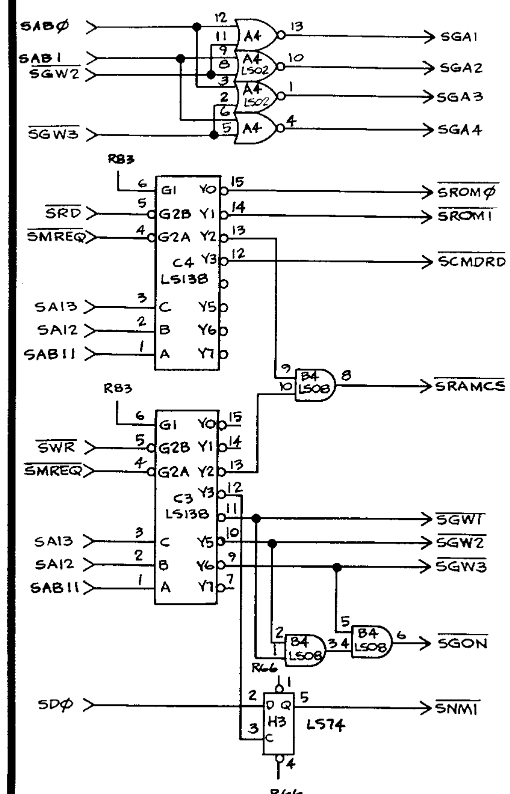
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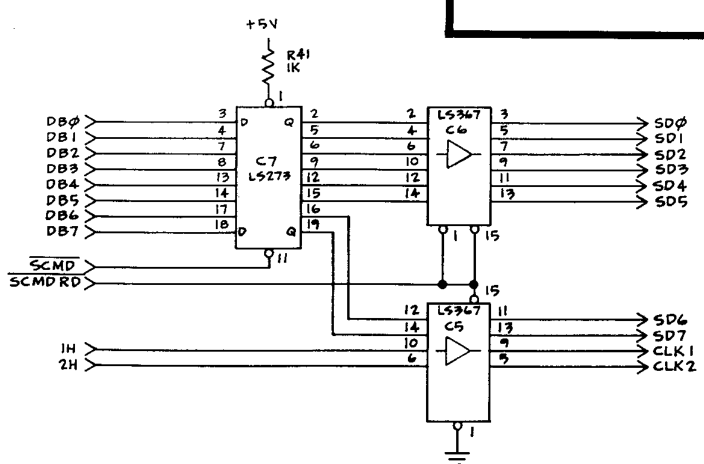
Sound Microprocessor



Sound Microprocessor Address Decoders



Sound Input



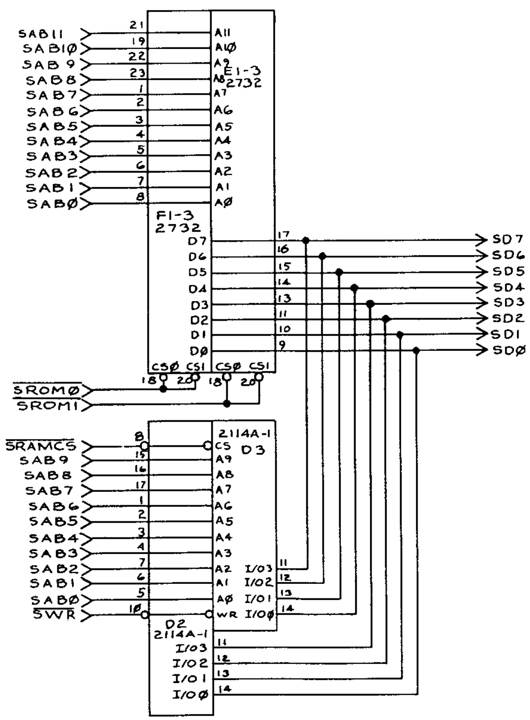
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Sound Input, Microprocessor, and Decoders

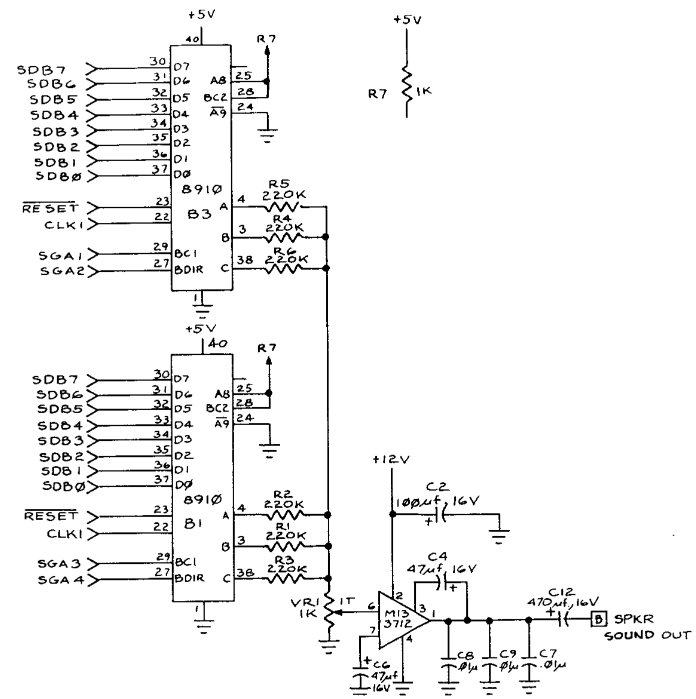
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Sound Memory



Sound Output



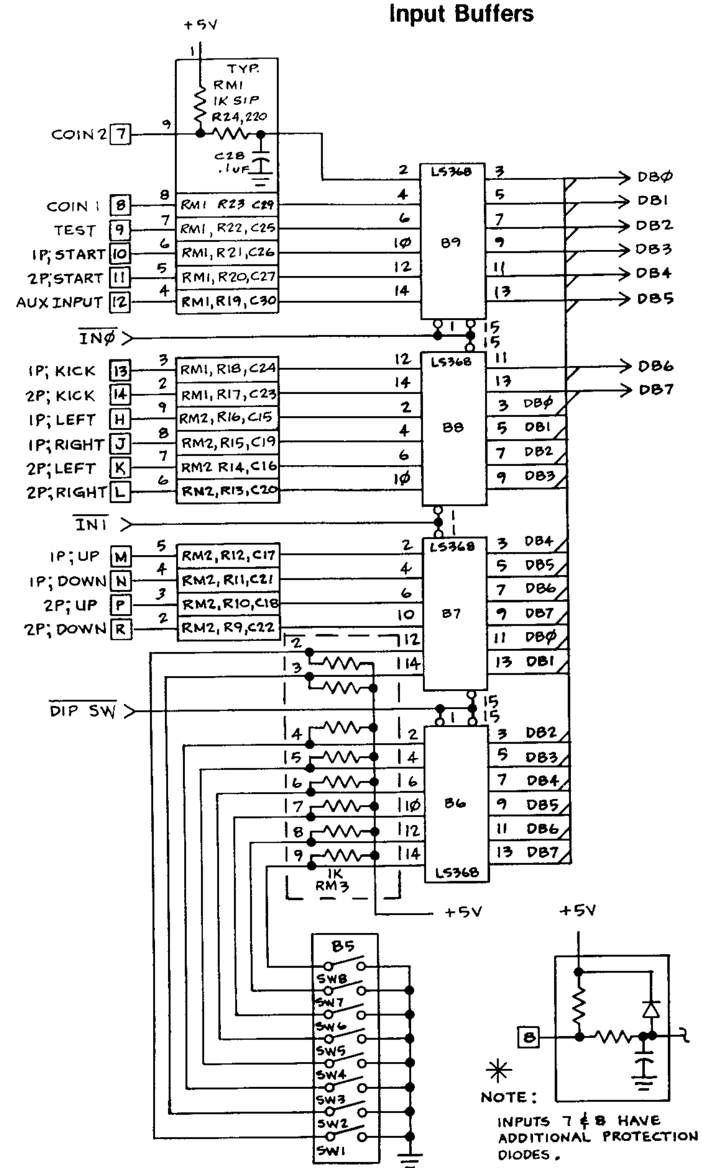
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Sound Memory and Output

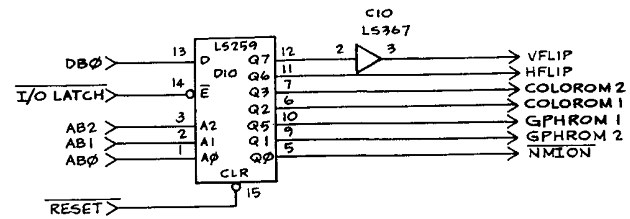
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Input Buffers



Control Signal Latch



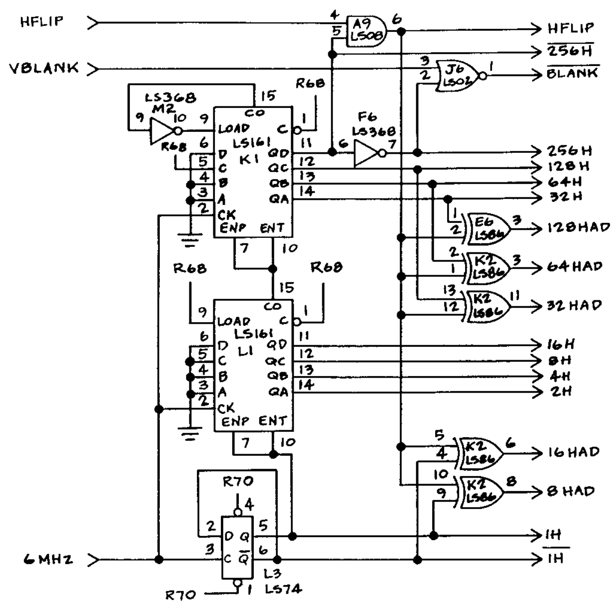
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Input Buffers and Control Signal Latch

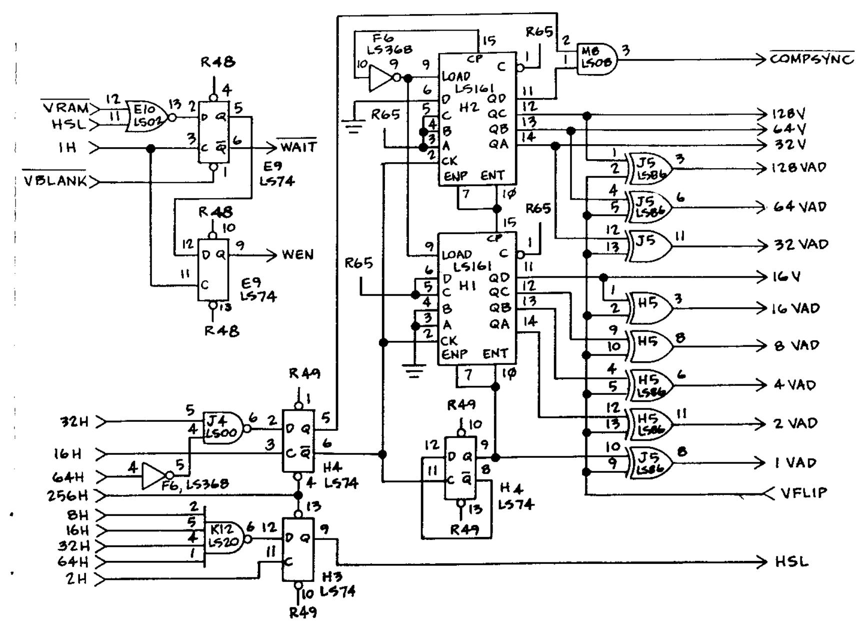
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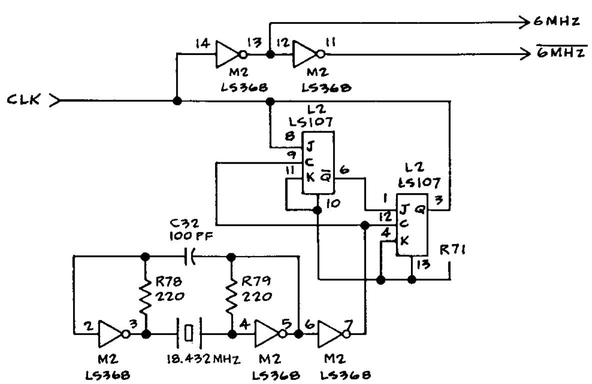
Horizontal Sync Chain



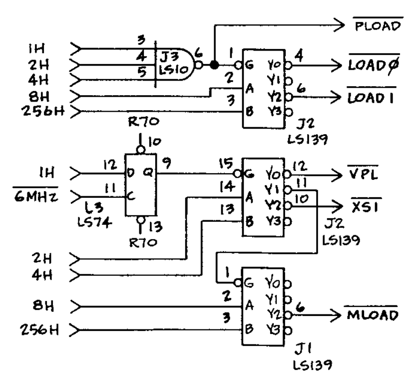
Vertical Sync Chain

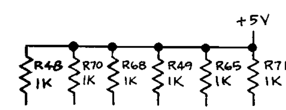


Crystal Clock



Control Load Signals





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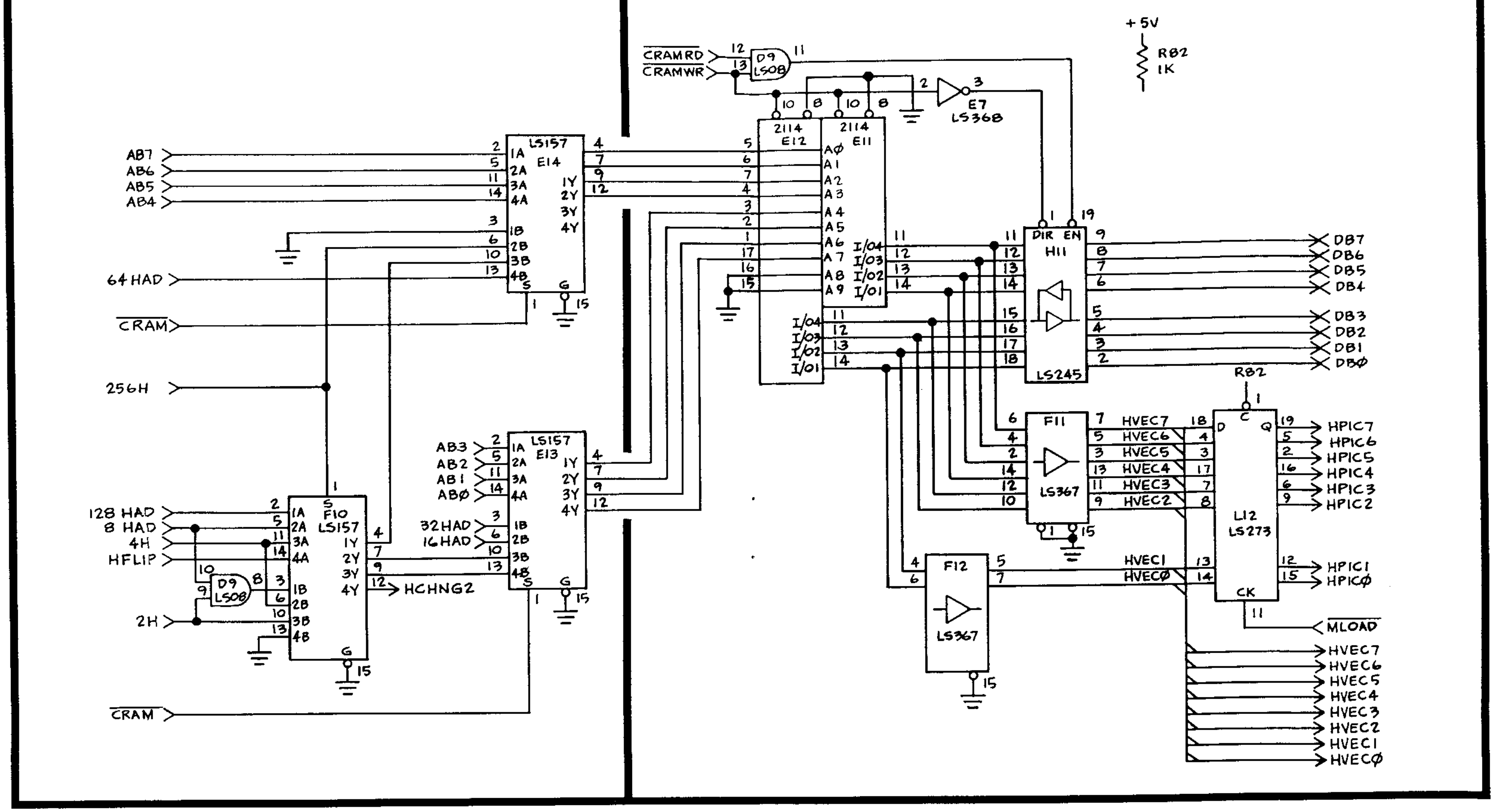
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Crystal Clock and Timing Chains

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Video Control RAM Address Multiplexers

Video Control RAM



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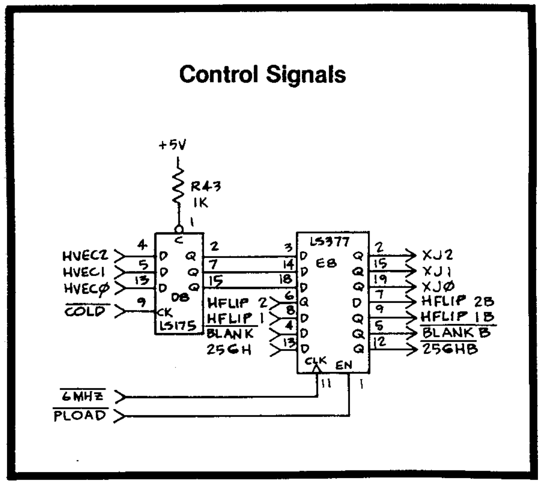
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Video Control Memory

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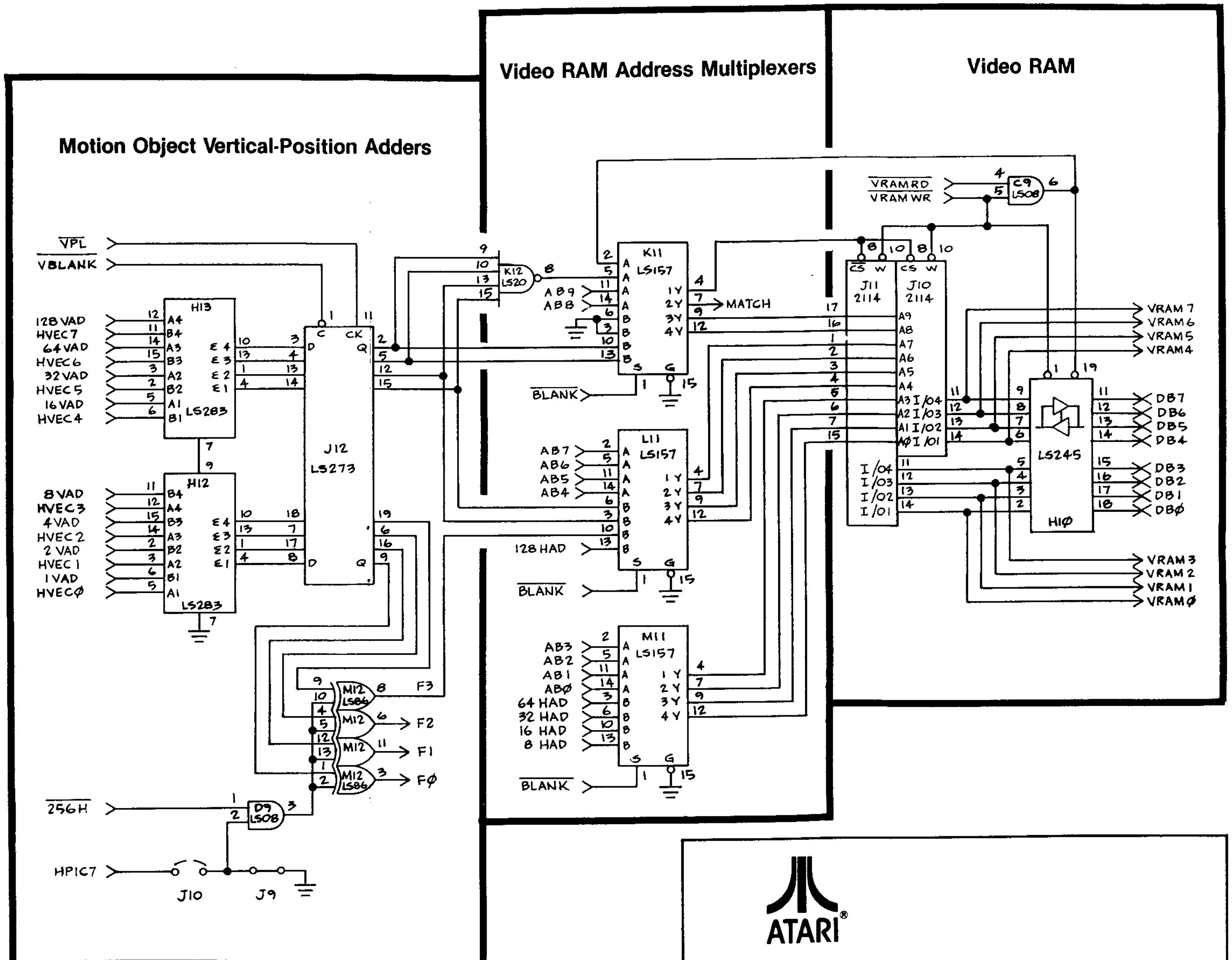
Control Signals



Motion Object Vertical-Position Adders

Video RAM Address Multiplexers

Video RAM

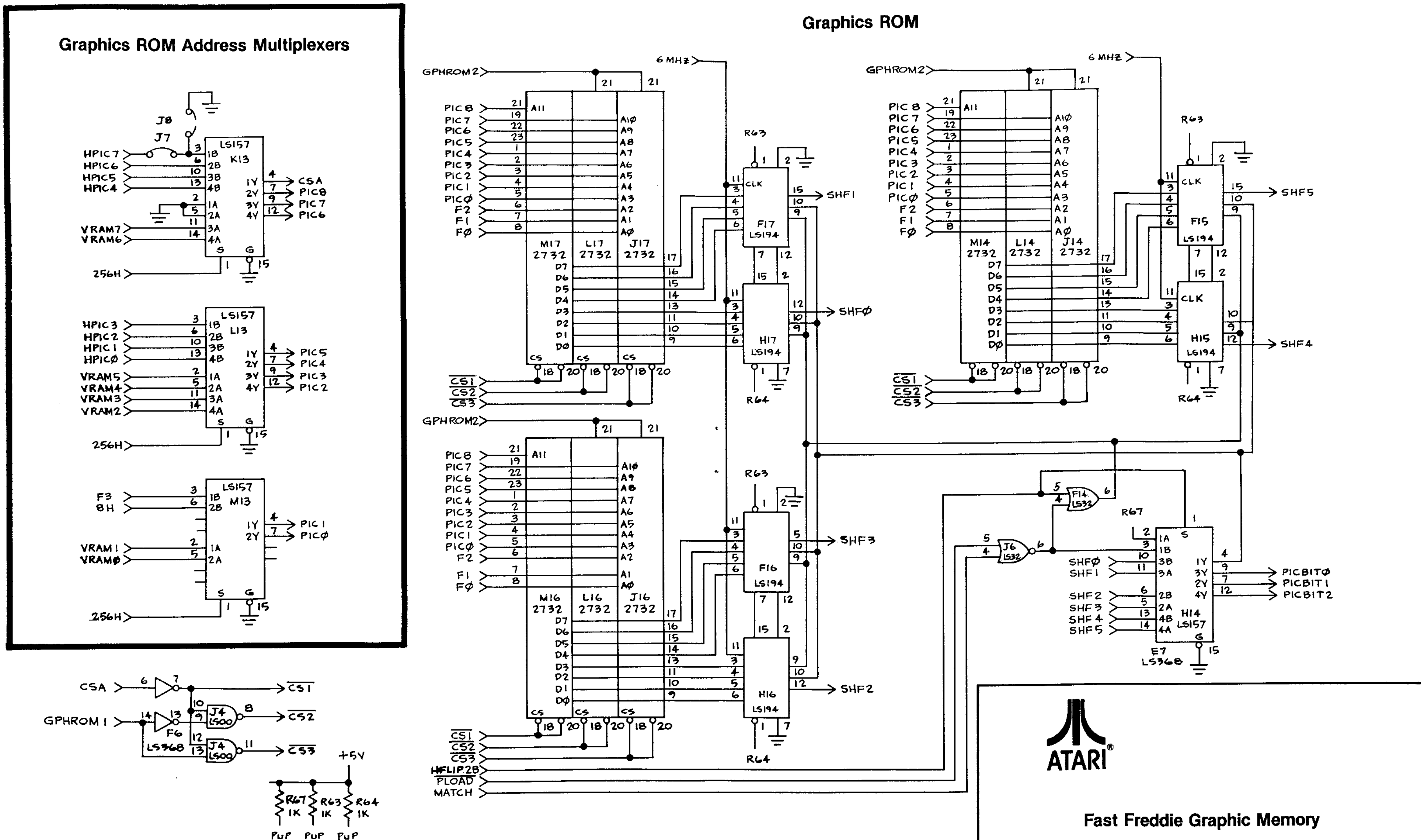


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Motion Object Logic and Video Memory

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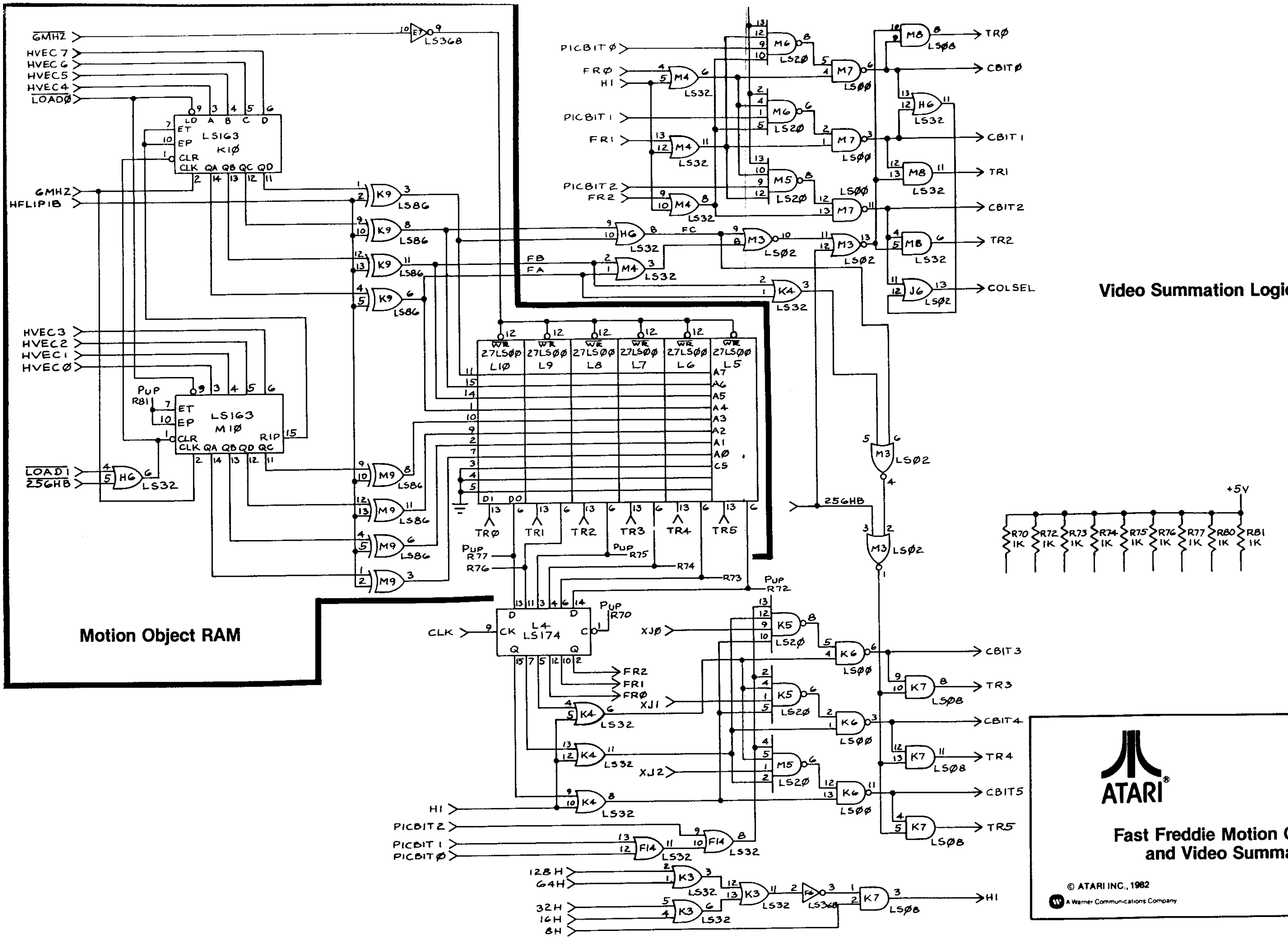
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Fast Freddie Graphic Memory

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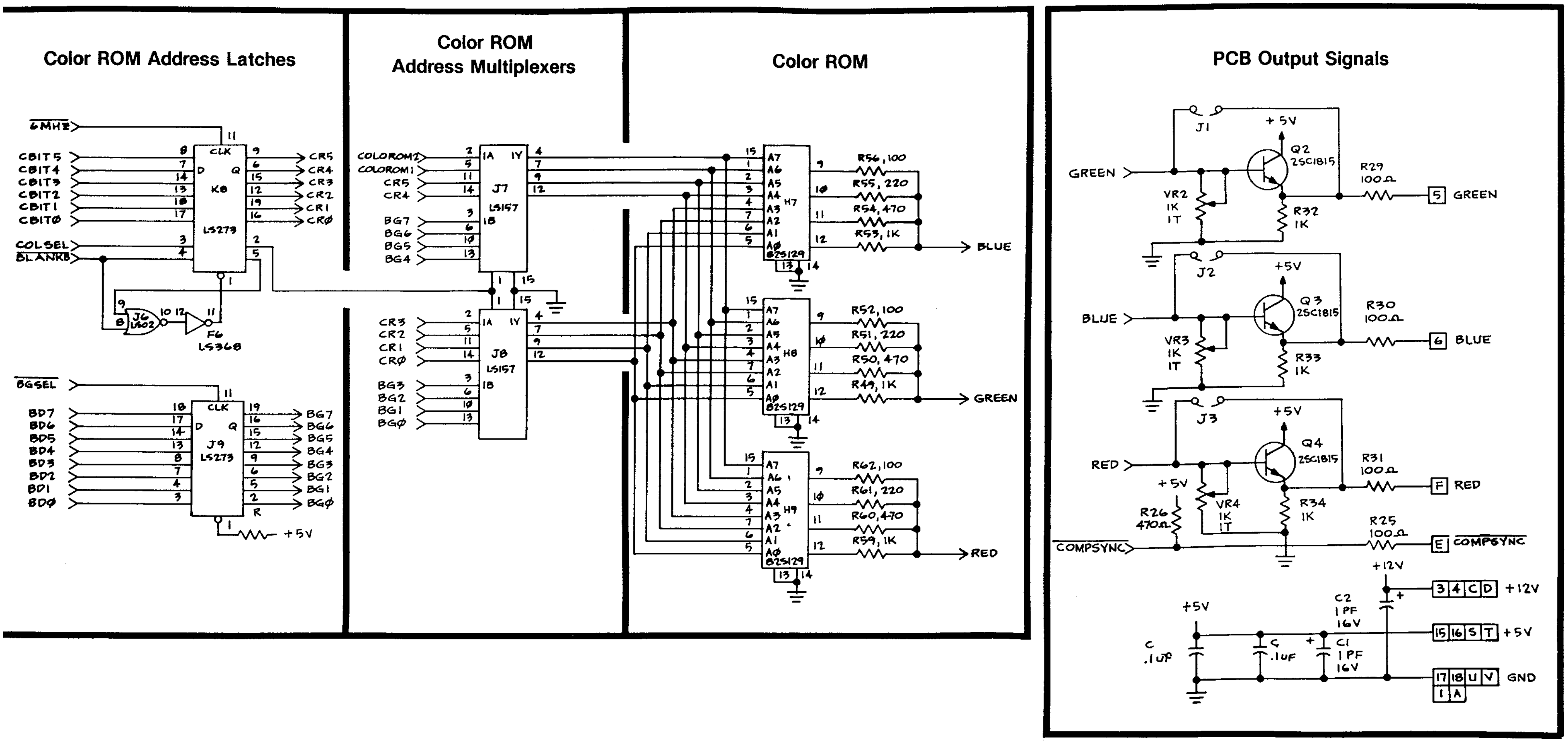


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Fast Freddie Motion Object Memory and Video Summation Logic

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Fast Freddie
Color Memory and PCB Outputs

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Descriptions of Signal Names for Fast Freddie PCB Schematic Diagrams

A12-A15

Game Microprocessor Address Lines 12-15 are generated by the Game Microprocessor (A & B 11/12). These signals are the select input signals for Game Microprocessor Address Decoders C11, C12, D11, D13, and for ROM Decoder A13.

AB0-AB11

Game Microprocessor Buffered Address Bus is generated by the Game Microprocessor (A & B 11/12), buffered by B13 and C13, and applied to the Program Memory, Video Control RAM Address Multiplexers, and Video RAM Address Multiplexers. AB0-AB2 are applied to D10. AB11 is applied to Game Microprocessor Address Decoders C11, C12, and D11.

BG0-BG7

Background Color Signals 0-7 are generated by Color ROM Address Latch J9. These signals are multiplexed with the CR0-CR5, COLOROM1, and COLOROM2 signals by Color ROM Address Multiplexers J7 and J8.

$\overline{\text{BGSEL}}$

Background Color Select is generated by Game Microprocessor Address Decoder D11 and applied as the clock input signal to Color ROM Address Latch J9.

$\overline{\text{BLANK}}$

Composite Blanking Signal is generated by logic gate J6 of the Horizontal Timing Chain and applied as the select input for Video RAM Address Multiplexers K11, L11, M11. $\overline{\text{BLANK}}$ is also applied to E8 to produce $\overline{\text{BLANKB}}$.

BLUE

Blue Video Output Signal is generated by Color ROM H7, buffered by Q3, and applied to the video display circuitry for further amplification and processing.

CBIT0-CBIT5

Color Bits 0-5 are generated by logic gates within K6 and M7 of the Video Summation Logic. They are then applied to the D input pins of Color ROM Address Latch K8 to produce CR0-CR5.

CLK

6-MHz Clock Signal is generated at pin 3 of J-K flip-flop L2 of the Crystal Clock circuit. CLK is used to clock the D-type flip-flops within L4 of the Video Summation Logic.

CLK1

Clock 1 is generated by driver C5 of the Sound Input circuit. This signal is derived from Horizontal Timing Signal 1H and is used to clock Programmable Sound Generators B1 and B3.

CLK2

Clock 2 is generated by driver C5 of the Sound Input circuit. This signal is derived from Horizontal Timing Signal 2H and is the phase 2 clock signal for Sound Microprocessor D4-D7.

$\overline{\text{COLD}}$

Color Load is generated by J2 and applied as the clock input signal for D8.

COLOROM1-COLOROM2

Color ROM Enables 1 and 2 are generated by Control Signal Latch D10 and applied to Color ROM Address Multiplexer J7.

COLSEL

Color Select is taken from logic gate J6 of the Video Summation Logic and applied through Color ROM Address Latch K8 to the select input pins of Color ROM Address Multiplexers J7 and J8.

$\overline{\text{COMPSYNC}}$

Composite Synchronization Signal is taken from logic gate M8 in the Vertical Timing Chain and applied to the video display circuitry for further processing.

CR0-CR5

Color Signals 0-5 are generated by Color ROM Address Latch K8 from signals CBIT0-CBIT5. CR0-CR5 are applied to Color ROM Address Multiplexers J7 and J8.

$\overline{\text{CRAM}}$

Control RAM Enable is generated by Game Microprocessor Address Decoder C12 and applied as the select input to Video Control RAM Address Multiplexers E13 and E14.

$\overline{\text{CRAMRD}}$

Control RAM Read is generated by Game Microprocessor Address Decoder C11 and applied through logic gate D9 as the read enable for the Video Control RAM.

$\overline{\text{CRAMWR}}$

Control RAM Write is generated by Game Microprocessor Address Decoder D11 and applied as the write enable for the Video Control RAM.

$\overline{\text{CS1}}$-$\overline{\text{CS3}}$

Graphics ROM Chip-Select Enables 1-3 are generated from the CSA and GPHROM1 signals by logic gates E7, F6, and J4 of the Graphics ROM circuit.

CSA

Graphics ROM Chip-Select Address is generated by Graphics ROM Address Multiplexer K13 and applied to logic gate E7 to develop $\overline{\text{CS1}}$-$\overline{\text{CS3}}$.

$\overline{\text{CSTMRD}}$

Custom RAM Read is generated by Game Microprocessor Address Decoder C11 and applied as the read enable for Custom RAM D16 and D17.

$\overline{\text{CSTMWR}}$

Custom RAM Write is generated by Game Microprocessor Address Decoder D11 and applied as the write enable for the Custom RAM D15 and D17.

D0-D7

Game Microprocessor Data Bus is a bi-directional data bus between the Game Microprocessor and the Program Memory.

DB0-DB7

Game Microprocessor Buffered Data Bus is a buffered bidirectional data bus between Game Microprocessor Data-Bus Buffer B10 and C7 of the Sound Input circuit, Input Signal Buffers B6-B9, buffer H11 of the Video Control RAM, buffer H10 of the Video RAM, and Color ROM Address Latch J9. DB0 is also applied to Control Signal Latch D10.

$\overline{\text{DIPSW}}$

Dip-Switch Read Enable is generated by Game Microprocessor Address Decoder C11 and applied as the read enable for Input Buffers B6 and B7.

GPHROM1-GPHROM2

Graphics ROM Enables 1 and 2 are generated by Control Signal Latch D10. GPHROM1 is used to develop $\overline{\text{CS1}}$-$\overline{\text{CS3}}$. GPHROM2 enables Graphics ROM J14, J17, L14, L17, M14, and M17.

GREEN

Green Video Output Signal is generated by Color ROM H8, buffered by Q2, and applied to the video display circuitry for further amplification and processing.

HFLIP

Horizontal Flip is generated by Control Signal Latch D10 and applied to logic gate A9 of the Horizontal Timing Chain to produce HFLIP1. HFLIP is also applied to Video Control RAM Address Multiplexer F10.

HFLIP1-HFLIP2

Horizontal Change Signals 1 and 2. HFLIP1 is generated by logic gate A9 of the Horizontal Timing Chain and buffered by E8 to produce HFLIP1B. HFLIP2 is generated by Video Control RAM Address Multiplexer F10 and buffered by E8 to produce HFLIP2B.

HFLIP1B-HFLIP2B

Buffered Horizontal Change Signals 1 and 2 are generated by E8 from HFLIP1 and HFLIP2. HFLIP1B is applied to logic gates K9 and M9 in the Motion Object RAM circuit to develop the input signals for Motion Object RAM L5-L10. HFLIP2B is applied to logic gate F14 of the Graphics ROM circuit to develop the S1 input signal for shift registers F15-F17 and H15-H17.

HPIC0-HPIC7

Horizontal Pictures 0-7 are generated by Video Control RAM L12 from the HVEC0-HVEC7 signals. The HPIC0-HPIC7 signals are applied to Graphic ROM Address Multiplexers K13 and L13. HPIC7 is applied through jumper J10 to logic gate D9 of the Motion Object Vertical Position Adders circuit.

HVEC0-HVEC7

Horizontal Vectors 0-7 are generated by F11 and F12 of the Video Control RAM and used by L12 to produce HPIC0-HPIC7. HVEC0-HVEC7 are also applied to H12 and H13 of the Motion Object Vertical Position Adders, and to K10 and M10 of the Motion Object RAM. HVEC0-HVEC2 are applied to D8.

$\overline{\text{IN0}}$-$\overline{\text{IN1}}$

Input Buffer Enables 0 and 1 are generated by Game Microprocessor Address Decoder C11 and applied to Input Buffers B7-B9.

$\overline{\text{I/O LATCH}}$

Input/Output Latch is generated by Game Microprocessor Address Decoder D11 and applied as the enable input signal for Control Signal Latch D10.

$\overline{\text{LOAD0}}$-$\overline{\text{LOAD1}}$

Horizontal Load Signals 0 and 1 are generated by J2 from the Horizontal Timing Signals. $\overline{\text{LOAD0}}$ is the load input signal for K10 and M10 of the Motion Object RAM. $\overline{\text{LOAD1}}$ is gated with Horizontal Timing Signal $\overline{\text{256HB}}$ by H6 to develop the clear input signal for K10 and M10 of the Motion Object RAM.

MATCH

Match is generated by Video RAM Address Multiplexer K11. MATCH is applied to the Graphics ROM circuit where it is gated with $\overline{\text{PLOAD}}$ by J6 to produce the S0 input signal for shift registers F15-F17 and H15-H17.

$\overline{\text{MLOAD}}$

Motion Object Load is generated by J1 and applied as the clock input signal to the D-type flip-flops within L12 of the Video Control RAM.

$\overline{\text{MREQ}}$

Game Microprocessor Memory Request is generated by the Game Microprocessor (A & B 11/12) and applied to Game Microprocessor Address Decoder D13.

$\overline{\text{NMION}}$

Non-Maskable Interrupt On is generated by Control Signal Latch D10 and applied to F5 to clear the non-maskable interrupt latch for the Game Microprocessor.

PIC0-PIC8

Picture Address Bits 0-8 are generated by Graphic ROM Address Multiplexers K13, L13, and M13. The PIC0-PIC8 signals are applied to Graphics ROM J14, J16, J17, L14, L16, L17, M14, M16, and M17.

PICBIT0-PICBIT2

Picture Bits 0-2 are generated by multiplexer H14 of the Graphics ROM circuit and applied to F14, M5, and M6 of the Video Summation Logic.

$\overline{\text{PLOAD}}$

Picture Load is generated by logic gate J3 and applied as the enable signal to E8. $\overline{\text{PLOAD}}$ is also applied to logic gate J6 of the Graphics ROM circuit.

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Fast Freddie
PCB Signal Name Glossary

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Descriptions of Signal Names for Fast Freddie PCB Schematic Diagrams (continued)

RAMSEL

RAM Select is generated by Game Microprocessor Address Decoder D13 and applied to Game Microprocessor Address Decoders C11, C12, and D11.

RD

Game Microprocessor Read is generated by the Game Microprocessor (A & B 11/12) and applied through driver C10 to Game Microprocessor Address Decoder C11, Game Microprocessor ROM Decoder A13, and to Data-Bus Buffer B10.

RDA

Game Microprocessor Read Enable is generated by logic gate D12 of the Game Microprocessor Address Decoder circuit. RDA is applied as the direction input signal for Data-Bus Buffer B10.

RED

Red Video Output Signal is generated by Color ROM H9, buffered by Q4, and applied to the video display circuitry for further amplification and processing.

RESET

Game Reset is generated by logic gates C8, E10, and F7 of the Game Microprocessor circuit from the WDR signal and the RESET switch. RESET is applied to the Game Microprocessor (A & B 11/12), Sound Microprocessor D4-D7, Programmable Sound Generators B1 and B3, and Control Signal Latch D10.

RFSH

Game Microprocessor Refresh is generated by the Game Microprocessor (A & B 11/12) and applied to Game Microprocessor Address Decoder C12.

ROM0-ROM7

Program ROM Chip-Select Enables 0-7 are generated by Game Microprocessor ROM Decoder A13 and applied to the Program ROM.

ROMSEL

Program ROM Select is generated by Game Microprocessor Address Decoder D13, gated by C9, and applied to Game Microprocessor ROM Decoder A13.

SA12-SA13

Sound Microprocessor Address Lines 12 and 13 are generated by Sound Microprocessor D4-D7 and applied to Sound Microprocessor Address Decoders C3 and C4.

SAB0-SAB11

Sound Microprocessor Buffered Address Bus is generated by Sound Microprocessor D4-D7, buffered by E4 and E5, and applied to the Sound Microprocessor Address Decoders and the Sound Memory.

SCMD

Sound Command is generated by Game Microprocessor Address Decoder D11 and applied as the clock input for the D-type flip-flops within C7 of the Sound Input circuit.

SCMDRD

Sound Command Read is generated by Sound Microprocessor Address Decoder C4 to enable drivers C5 and C6 of the Sound Input circuit.

SD0-SD7

Sound Microprocessor Data Bus is a bi-directional data bus between the Sound Microprocessor and Sound Memory D2-D3, E1-E3, F1-F3 and Sound Input buffers C5C6. SD0 is applied to Sound Microprocessor Address Decoder H3 to produce SNMI.

SDB0-SDB7

Sound Microprocessor Buffered Data Bus is a buffered bi-directional data bus between Sound Microprocessor Data-Bus Buffer C2 and Programmable Sound Generators B1 and B3.

SGA1-SGA4

Programmable Sound Generator Control Lines 1-4 are generated by the logic gates within A4 of the Sound Microprocessor Address Decoder circuit and applied to Programmable Sound Generators B1 and B3.

SGON

Programmable Sound Generator Write Enable is generated by logic gate B4 of the Sound Microprocessor Address Decoder circuit and applied to Sound Microprocessor Data-Bus Buffer C2.

SGW1-SGW3

Sound Generator Control Lines 1-3 are generated by Sound Microprocessor Address Decoder C3 and applied to logic gate B4 to produce SGON. SGW2 and SGW3 are also applied to logic gate A4 to produce SGA1-SGA4.

SHF0-SHF5

Pixel Bits 0-5 are generated by shift registers F15-F17 and H15-H17 of the Graphics ROM circuit and applied to multiplexer H14 to produce PICBIT0-PICBIT2.

SMREQ

Sound Microprocessor Memory Request is generated by Sound Microprocessor D4-D7 and applied to Sound Microprocessor Address Decoders C3 and C4.

SNMI

Sound Microprocessor Non-Maskable Interrupt is generated by H3 of the Sound Microprocessor Address Decoder circuit and applied to F4 to clear the nonmaskable interrupt latch for the Sound Microprocessor.

SRAMCS

Sound RAM Chip Select is generated by logic gate B4 of the Sound Microprocessor Address Decoder circuit and applied to Sound Memory D2 and D3.

SRD

Sound Microprocessor Read is generated by Sound Microprocessor D4-D7 and applied to Sound Microprocessor Address Decoder C4.

$\overline{\text{SROM0}}$-$\overline{\text{SROM1}}$

Sound ROM Chip-Select Enables 0-1 are generated by Sound Microprocessor Address Decoder C4 and applied as the select input signals to Sound Memory E1-E3 and F1-F3.

$\overline{\text{SWR}}$

Sound Microprocessor Write is generated by Sound Microprocessor D4-D7 and applied to Sound Microprocessor Address Decoder C3 and to Sound Memory D2-D3.

VBLANK

Vertical Blanking (active HIGH) is generated by F5 of the Game Microprocessor circuit and applied to logic gate J6 of the Horizontal Timing Chain to produce BLANK.

$\overline{\text{VBLANK}}$

Vertical Blanking (active LOW) is generated by F5 of the Game Microprocessor circuit and applied as the clock input signal to counter C8 of the Game Microprocessor circuit. $\overline{\text{VBLANK}}$ is also applied as the clear input signal to C10 and to the D-type flip-flops within J12 of the Motion Object Vertical Position Adders circuit.

VFLIP

Vertical Flip is generated by Control Signal Latch D10 and applied through driver C10 to logic gates H5 and J5 of the Vertical Timing Chain.

VPL

Vertical Position Load is generated by J2 and applied as the clock input signal for the D-type flip-flops of J12 in the Motion Object Vertical Position Adders circuit.

$\overline{\text{VRAM}}$

Video RAM Enable is generated by Game Microprocessor Address Decoder C12 and applied to logic gate B11.

VRAM0-VRAM7

Video RAM Output Data 0-7 is generated by Video RAM J10 and J11 and applied to Graphics ROM Address Multiplexers K13, L13, M13.

$\overline{\text{VRAMRD}}$

Video RAM Read is generated by Game Microprocessor Address Decoder C11 and gated with $\overline{\text{VRAMWR}}$ by C9 of the Video RAM circuit to produce the read enable signal for H10 and K11.

$\overline{\text{VRAMWR}}$

Video RAM Write is generated by Game Microprocessor Address Decoder D11 and gated with $\overline{\text{VRAMRD}}$ by C9 of the Video RAM circuit to produce the write enable signal for H10 and K11. $\overline{\text{VRAMWR}}$ is also the write enable signal for Video RAM J10 and J11.

$\overline{\text{WAIT}}$

Game Microprocessor Wait is generated by C10 and applied as the wait input signal to the Game Microprocessor (A & B 11/12).

$\overline{\text{WDR}}$

Watchdog Reset is generated by Game Microprocessor Address Decoder C11 and applied to logic gate F7 of the Game Microprocessor circuit.

WEN

Write Enable is generated by C10 and applied to Game Microprocessor Address Decoder D11.

$\overline{\text{WR}}$

Game Microprocessor Write is generated by the Game Microprocessor (A & B 11/12), buffered by logic gate C10, and applied to Game Microprocessor Address Decoder D11 and to Custom RAM D15-D17.

$\overline{\text{WRKRAM}}$

Working RAM Enable is generated by logic gate C9 of the Game Microprocessor Address Decoder circuit and applied to Custom RAM F15-F17.

1H-256H, $\overline{\text{1H}}$, $\overline{\text{256HB}}$

Horizontal Timing Signals are generated by the Horizontal Timing Chain and used throughout the game circuitry.

8HAD-128HAD

Horizontal Address Signals are generated by the Horizontal Timing Chain and applied to Video Control RAM Address Multiplexers E13, E14, F10, and to Video RAM Address Multiplexers L11 and M11.

$\overline{\text{6 MHZ}}$, 6 MHZ

6-MHz Timing Signals are generated by the Crystal Clock circuit and used throughout the game circuitry.

16V-128V

Vertical Timing Signals are generated by the Vertical Timing Chain and applied to J3 and F5 of the Game Microprocessor circuit and to J4 and F4 of the Sound Microprocessor circuit.

1VAD-128VAD

Vertical Address Signals are generated by the Vertical Timing Chain and applied to Motion Object Vertical Position Adders H12 and H13.

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Fast Freddie
PCB Signal Name Glossary (continued)

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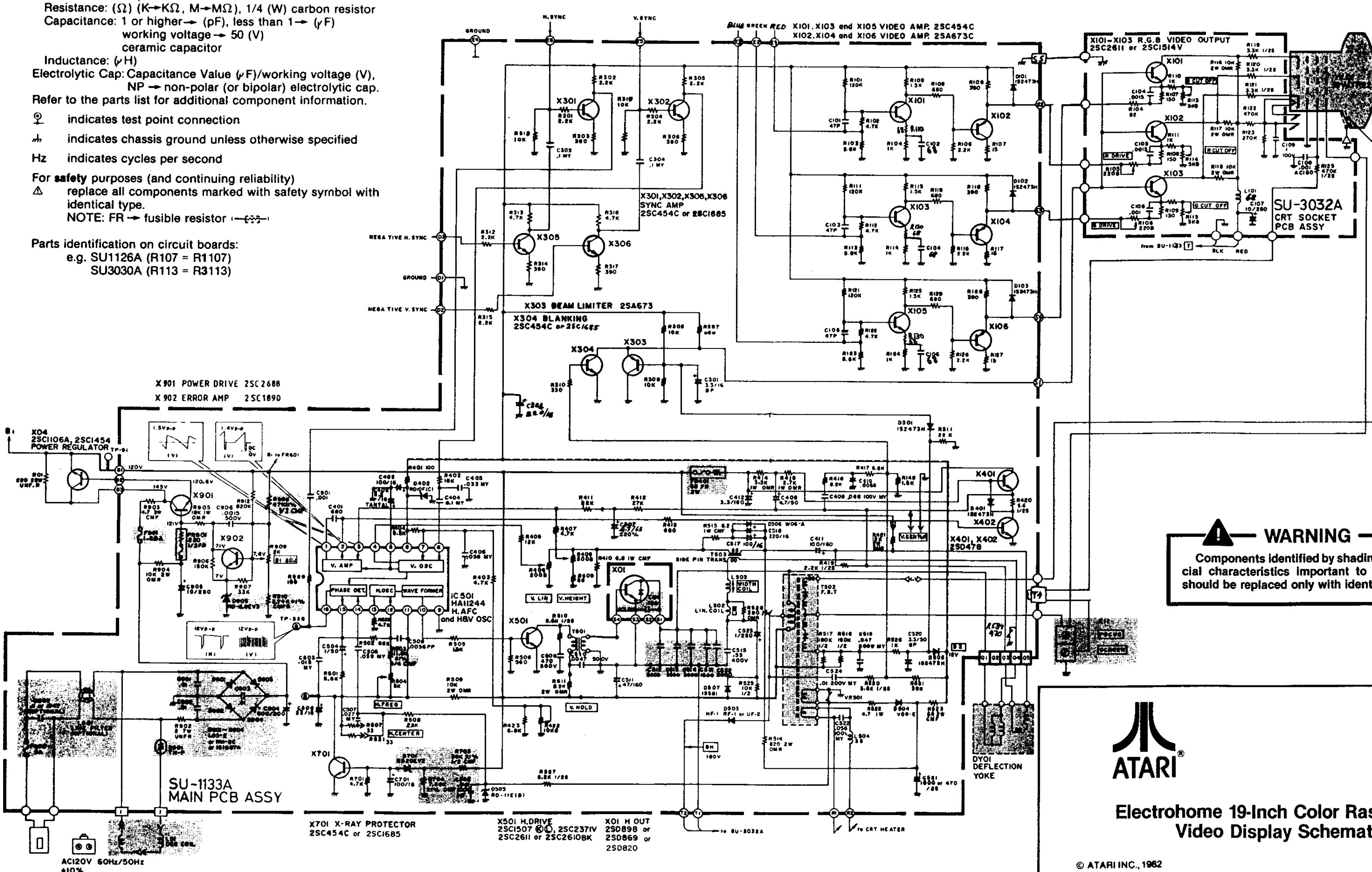
Schematic Notes
Unless otherwise specified
Resistance: (Ω) (K→KΩ, M→MΩ), 1/4 (W) carbon resistor
Capacitance: 1 or higher→ (pF), less than 1→ (μF)
working voltage→ 50 (V)
ceramic capacitor
Inductance: (μH)
Electrolytic Cap: Capacitance Value (μF)/working voltage (V),
NP → non-polar (or bipolar) electrolytic cap.
Refer to the parts list for additional component information.

indicates test point connection
indicates chassis ground unless otherwise specified
Hz indicates cycles per second

For **safety** purposes (and continuing reliability)
⚠ replace all components marked with safety symbol with identical type.
NOTE: FR → fusible resistor

Parts identification on circuit boards:
e.g. SU1126A (R107 = R1107)
SU3030A (R113 = R3113)

Electrohome 19-Inch Color Raster-Scan Video Display Schematic Diagram



⚠ WARNING ⚠

Components identified by shading have special characteristics important to safety and should be replaced only with identical types.

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Electrohome 19-Inch Color Raster-Scan Video Display Schematic

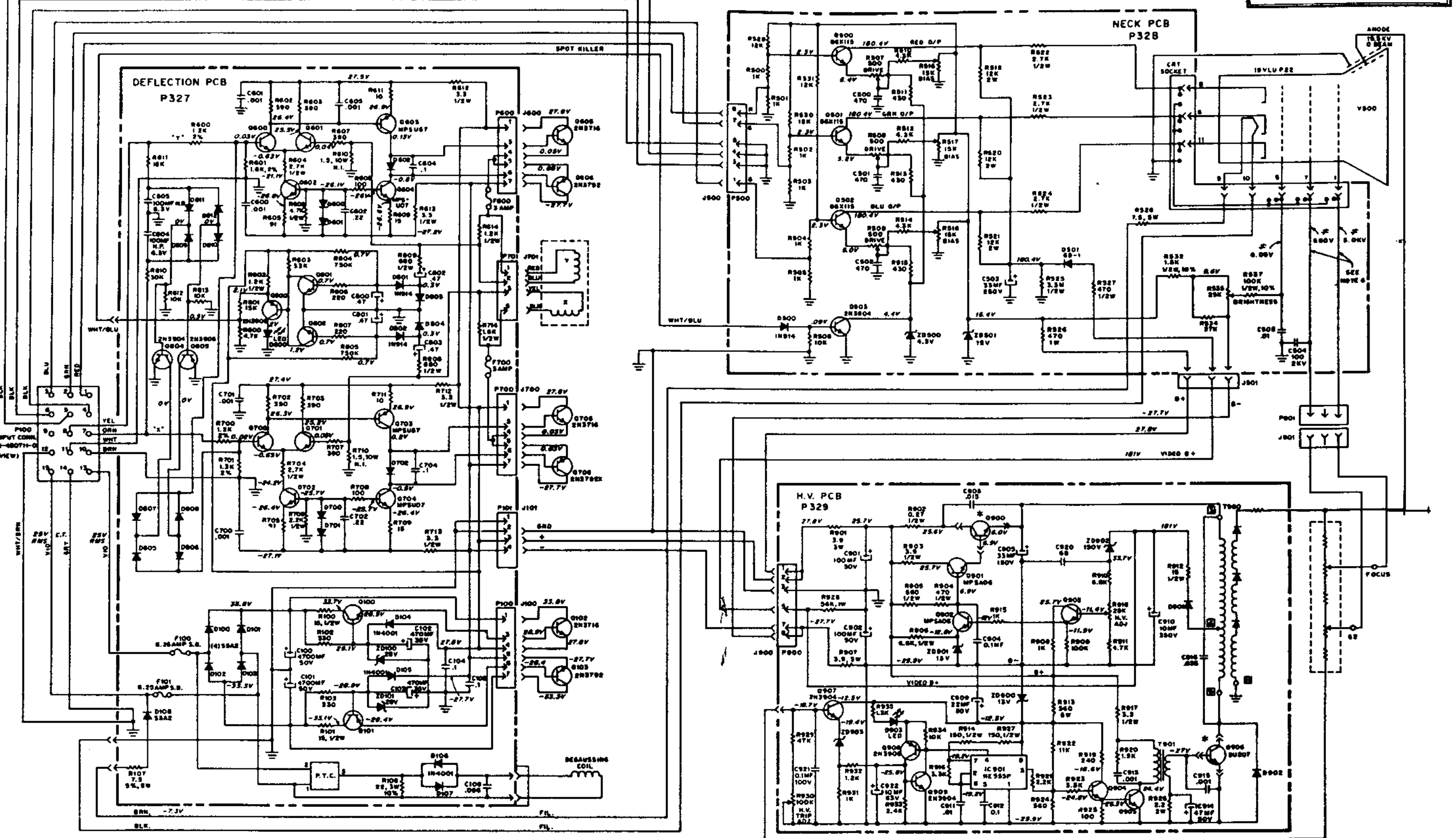
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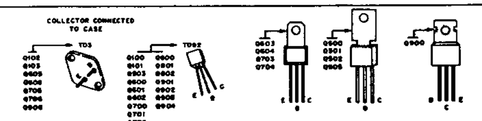
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19" COLOR GRAPHIC DISPLAY SCHEMATIC DIAGRAM

WELLS-GARDNER ELECTRONICS CORP.
CHICAGO, ILLINOIS 60639
TELEPHONE (312) 252-8220





GENERAL NOTES:

1. RESISTANCE VALUES IN OHMS 1/4 WATT, 5% UNLESS OTHERWISE NOTED. K=1,000, M=1,000,000
2. CAPACITANCE VALUE OF 1 OR LESS IN MICROFARADS, ABOVE 1 IN PICOFARADS UNLESS OTHERWISE NOTED.
3. * Q900 AND Q906 ARE NOT ON H.V.P.C.B.
4. ALL D.C. VOTAGES 10% MEASURED FROM POINT INDICATED TO GROUND USING A HIGH IMPEDANCE METER. VOLTAGES ARE MEASURED WITH NO SIGNAL INPUT AND CONTROLS ARE IN A NORMAL OPERATING POSITION
5. CIRCLED NUMBERS INDICATE LOCATION OF WAVE-FORM READING.
6. USE A 1,000:1 PROBE WHEN MEASURING SCREEN OR FOCUS VOLTAGE.
7. # VOLTAGES VARY WITH CONTROL SETTINGS.

19K6102-5835

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Wells-Gardner 19-Inch Color Raster-Scan Video Display Schematic

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